AMENDMENTS TO THE CLAIMS

Claim 1. (currently amended) Channel decoder for a digital broadcast receiver, comprising a synchronization byte detector (1) for detecting synchronization bytes in a decoded transmission signal, **characterized in that** said synchronization byte detector (1) provides a synchronization signal indicating a start of frame for transport stream packets in the decoded transmission signal and a lock detected output signal indicating the lock-in of the receiver to one broadcast channel which is used as a feed forward and/or feed back signal to respectively switch processing stages succeeding and/or preceding said synchronization byte detector (1) into a different mode dependent on whether or not lock has been achieved.

Claim 2. (original) Channel decoder according to claim 1, **characterized in that** a clock and/or carrier recovery circuit (2) preceding the synchronization byte detector (1) gets switched from a robust mode used for acquisition of a broadcast channel to a locked mode used in case only small deviations of an acquired broadcast channel need to be compensated in case of lock-in of the receiver and vice-versa in case the receiver is not locked-in.

Claim 3. (previously presented) Channel decoder according to claim 1, **characterized in that** the loop bandwidth of a clock and/or carrier recovery loop within the clock and/or carrier recovery circuit (2) gets switched from a wide bandwidth mode that allows the fast coarse lock of the receiver to the clock and/or carrier of a transmission signal to a narrow bandwidth mode which performs a low noise fine adjustment of the receiver to the clock and/or carrier of the transmission signal in case of lock-in of the receiver and vice-versa in case the receiver is not locked-in.

Claim 4. (previously presented) Channel decoder according to claim 1, **characterized in that** an adaptive equalizer (5b) within the channel decoder gets switched from an acquisition mode to a tracking mode in case of lock-in of the receiver and vice-versa in case the receiver is not locked-in.

Claim 5. (previously presented) Channel decoder according to claim 1, **characterized in that** a forward error correction stage (3, 6, 7) succeeding the synchronization byte detector (1) is switched from an off mode to an on mode in case of lock-in of the receiver and vice-versa in case the receiver is not locked-in.

Claim 6. (original) Channel decoder according to claim 5, **characterized in that** all stages succeeding the forward error correction stage (3, 6, 7) are switched from an off mode to on mode in case of lock-in of the receiver and vice-versa in case the receiver is not locked-in.

Claim 7. (previously presented) Channel decoder according to claim 1, **characterized by** an output port (4) to output said lock detected output signal to other processing stages within the receiver.

Claim 8. (previously presented) Channel decoder according to claim 1, **characterized in that** it is used in a DVB or a DAB receiver.

Cl cont.

Claim 9. (previously presented) Channel decoder according to claim 1, **characterized in that** it is used for satellite, cable or terrestrial reception.